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A new gate drive for a single-phase matrix converter

Rahimi Baharom[1], Nor Farahaida Abdul Rahman[2], Muhamad Nabil Hidayat[3], Khairul Safuan Muhammad[4], Mohammad Nawawi Seroji[5], Nor Zaihar Yahaya[6]
[1,2,3,4,5] Faculty of Electrical Engineering, Universiti Teknologi MARA, Malaysia.
[6] Department of Electrical & Electronics Engineering, Universiti Teknologi PETRONAS, Malaysia

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ABSTRACT

This paper presents the new generation of advanced gate driver circuit based on IR2110 device for a Single-Phase Matrix Converter (SPMC) circuit topology that uses MOSFETs or IGBTs switches. The new generation of gate drive circuit uses less number of components, since a single IR2110 device can drive two power switches, thus reduce power losses and minimize the complexity of conventional circuit. An additional isolation of the upper and lower sides of IR2110 device features additional protection to the proposed gate drive system. As a result, the proposed gate drive circuit just uses four IR2110 gate drives in order to control eight switches of SPMC circuit, thus, solve the conventional bulky gate drive circuit problem in SPMCs operation. This is in line with the international power electronic technology road-maps to reduce losses, cost, volume, therefore to raise up the power density of power electronics converters. Validation have been done through the experimental test-rig. As a result, such new theoretical enhancements can be used as a novel foundation of future high power density of SPMC circuit topology and in-line with the Fourth Industrial Revolution (IR 4.0) which were characterized mainly by advances in technology.

Corresponding Author:

Rahimi Baharom,
Faculty of Electrical Engineering,
Universiti Teknologi MARA,
40450 Shah Alam, Selangor, Malaysia.
Email: rahimi6579@gmail.com

1. INTRODUCTION

Matrix Converters (MC) have been classified as an advanced and emerging converter [1-2]. The SPMC as shown in Figure 1 consists of four bi-directional switches that interface with their input and output terminals [3-11]. In order to fulfil the design of high performance and high-speed switching applications, IGBTs or MOSFETs have been employed. Figure 2 shows the topology of S1 and S2 using IGBTs connected in common-emitter (common-E) [12-13]. Since the SPMC uses eight switches, hence, it requires eight gate driver circuits. The use of high-power transistors could lead to the use of gate drive circuits with a function of power amplifier that can accept low-power input for producing high voltage drive output. Gate drivers can be provided either on-chip or as a discrete module.

A conventional gate drive circuit is only capable to control a single switch, resulting in bulky conversion system [14-17]. It also requires several numbers of electronic components; thus, it could lead to high losses and reduces the efficiency of the SPMC system. Moreover, additional protection devices are required in order to protect the power switches. Recently, power electronic converters size and weight are critical when space is constraints [18-19]. Therefore, an alternative technology to solve the aforementioned problems are desirable. In this paper, a new gate drive based IR2110 is proposed for the SPMC circuit

topology; to increase the SPMC power density. It inherits simple circuit design with less number of devices used. Thus, it may solve the size and losses issues in SPMC. Therefore, the new gate drive circuit is in line with the power electronics technology roadmap that tends to reduce size, volume, losses and cost of future power converter [20].

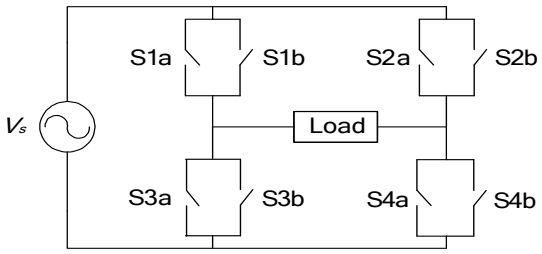

Figure 1. SPMC circuit topology

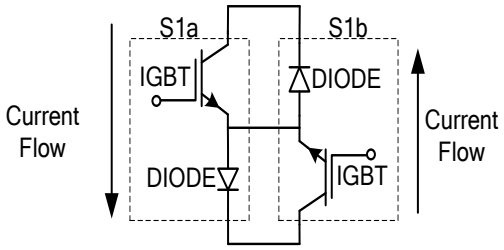

Figure 2. Switches arrangement

2. THE PROPOSED GATE DRIVE CIRCUIT FOR SPMC

The device of IR2110 at the heart of the second generation of gate drive circuit can with stand up to 500 V [21-24]. The proposed gate drive based on IR2110 allows a low current output signal from a 5 V signal generated by a microprocessor or microcontroller to drive MOSFETs and IGBTs operation. The IR2110 driver consists of a level-shifting circuitry and a bootstrap circuit to allow the power switches to turn ON. Additionally, the gate capacitance of MOSFETs or IGBTs need to be charged and discharged for them to turn ON and turn OFF respectively. Higher current provides to the gate (sink/source) will cause the switching activity of MOSFETs or IGBTs become faster. To avoid the risk of damaging the MOSFET, the gate drive must be designed to supply low current at appropriate voltage level.

Figure 3 shows the experimental test-rig and the schematic diagram of the advance gate drive system. The IR2110 device receives input signals in a form of Pulse Width Modulation (PWM) through the pin 12 for low side input and the pin 10 for high side input signals. These IR2110 are connected to the DC supply voltage through an isolated NMA0515 device [21]. The IR2110 will boost the input signal of the control circuit is from 5 V, to the output of 15 V. The TC4422 device is used to filter the noise and for soft driver operation. The use of the proposed drive circuit will cut the number of required drive circuits of the SPMC from eight to 4 circuits only. Thus, it reduces the number of components and circuit complexities for achieving low power losses and high-power density system [25].

Table 1 shows the number of gate drive circuits that connected to the HIGH and LOW sides terminals of the SPMC circuit topology; they are labelled as S1a, S1b, S2a, S2b, S3a, S3b, S4a, S4b. Switches that have been connected to the HIGH side terminal are S1a, S1b, S2a and S2b, while switches that have been connected to the LOW side terminal are S3a, S3b, S4a and S4b. So, for the gate drive 1, it has been connected to the pair of switches S1a and S3a. Meanwhile, the gate drive 2, has been connected to the pair of switches S1b and S3b. Then, for the gate drive 3, it has been connected to the pair of switches S2a and S4a. Lastly, the gate drive 4 has been connected to the pair of switches S2b and S4b.

Table 1. Circuit Arrangement

Sides	Gate Drive 1	Gate Drive 2	Gate Drive 3	Gate Drive 4
HIGH	S1a	S1b	S2a	S2b
LOW	S3a	S3b	S4a	S4b

3. RESULTS AND DISCUSSIONS

Figure 4 shows the experiment result of the output PWM signal. In order to verify the proposed gate drive circuit for the SPMC circuit topology, a simple inverter operation has been tested. The PWM signals (PWM 1 and PWM 2) are fed to the MOSFETs according to the switching algorithms tabulated in Table 2. The output voltage waveform for the inverter operation is as shown in Figure 5. It shows that the output AC voltage waveform follows the shape of the PWM signals. In addition, the frequency of the output AC voltage waveform can be directly controlled by varying the frequency of the PWM signals. In this work, the maximum frequency of the proposed gate drive circuit can be increased up to 100 kHz. Thus, it is suitable for medium and high frequency power electronics converters operation.

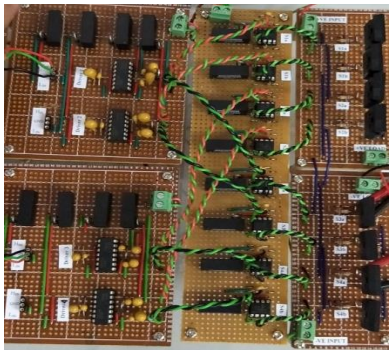

Figure 3. Circuit arrangement for experimental test-rig

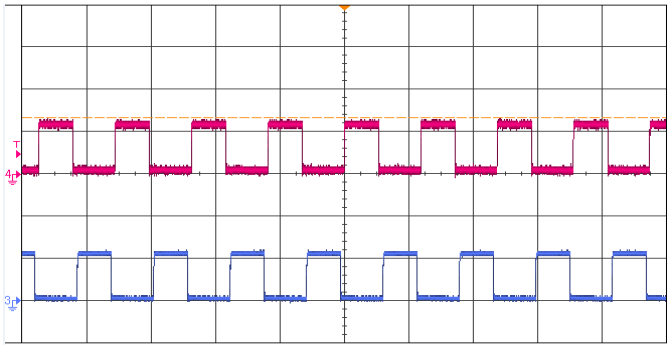

Figure 4. Experimental result of the output PWM signal for the proposed of gate drive circuit. (Scale: X axis: 15V/div, Y axis: 50µs/div)

Table 2. Switching algorithms for the DC to AC converter of the SPMC circuit topology

Mode of Operation	Switches	PWM Operation
Positive cycle	S1a	PWM 1
-	S1b	OFF
-	S2a	OFF
Negative cycle	S2b	PWM 2
-	S3a	OFF
Negative cycle	S3b	PWM 2
Positive cycle	S4a	PWM 1
-	S4b	OFF

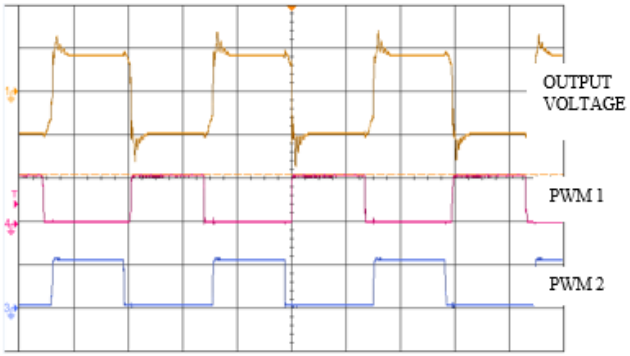

Figure 5. Experimental result of the output voltage waveform for the DC to AC converter of the SPMC circuit topology (Scale: X axis: 15V/div, Y axis: 20µs/div)

4. CONCLUSION

The new generation of advanced gate drive circuit that could reduce the number of components used, thus, increase the power density of SPMC circuit has been presented. This is in line with the increasing demand for smaller size, light in weight and high efficiency converters in recent years, caused by the continual development of power density for power electronic converters. The proposed gate drive circuit capable to enhance the reliability of the SPMC circuit. Additional isolation between high and low sides of power switches connection from IR2110 devices could lead to high robustness performance of the proposed system.

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